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DETECTING OVER PROGRAMMED MEMORY
Chen, et al.
Unknown
Herewith
EV 332 013 511 US

Docket No.:
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Burt Magen
(415) 369-9660

Fig. 1

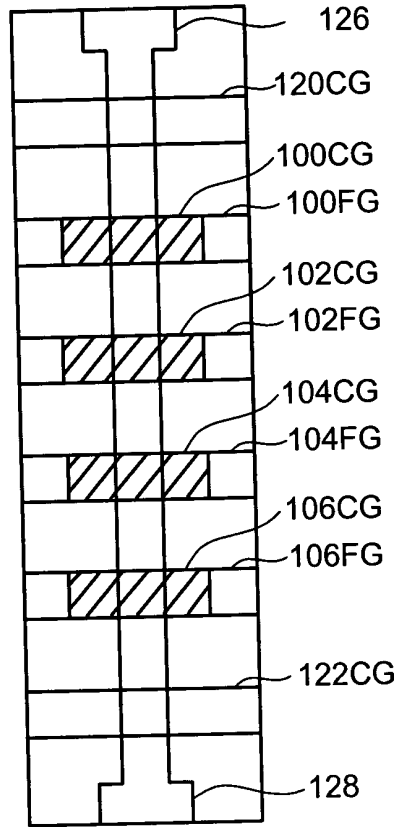


Fig. 2

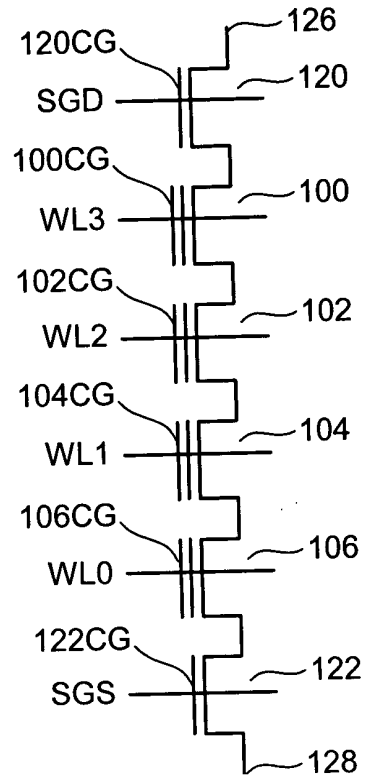
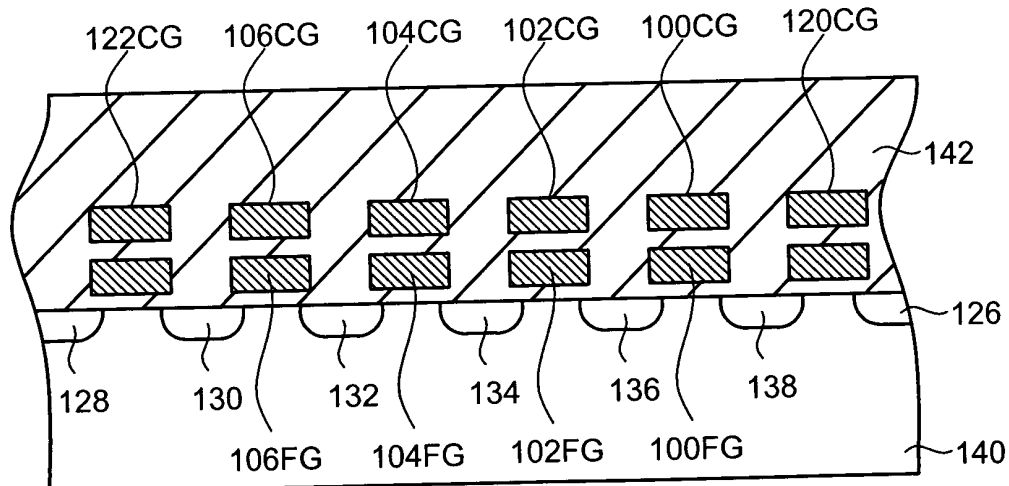


Fig. 3



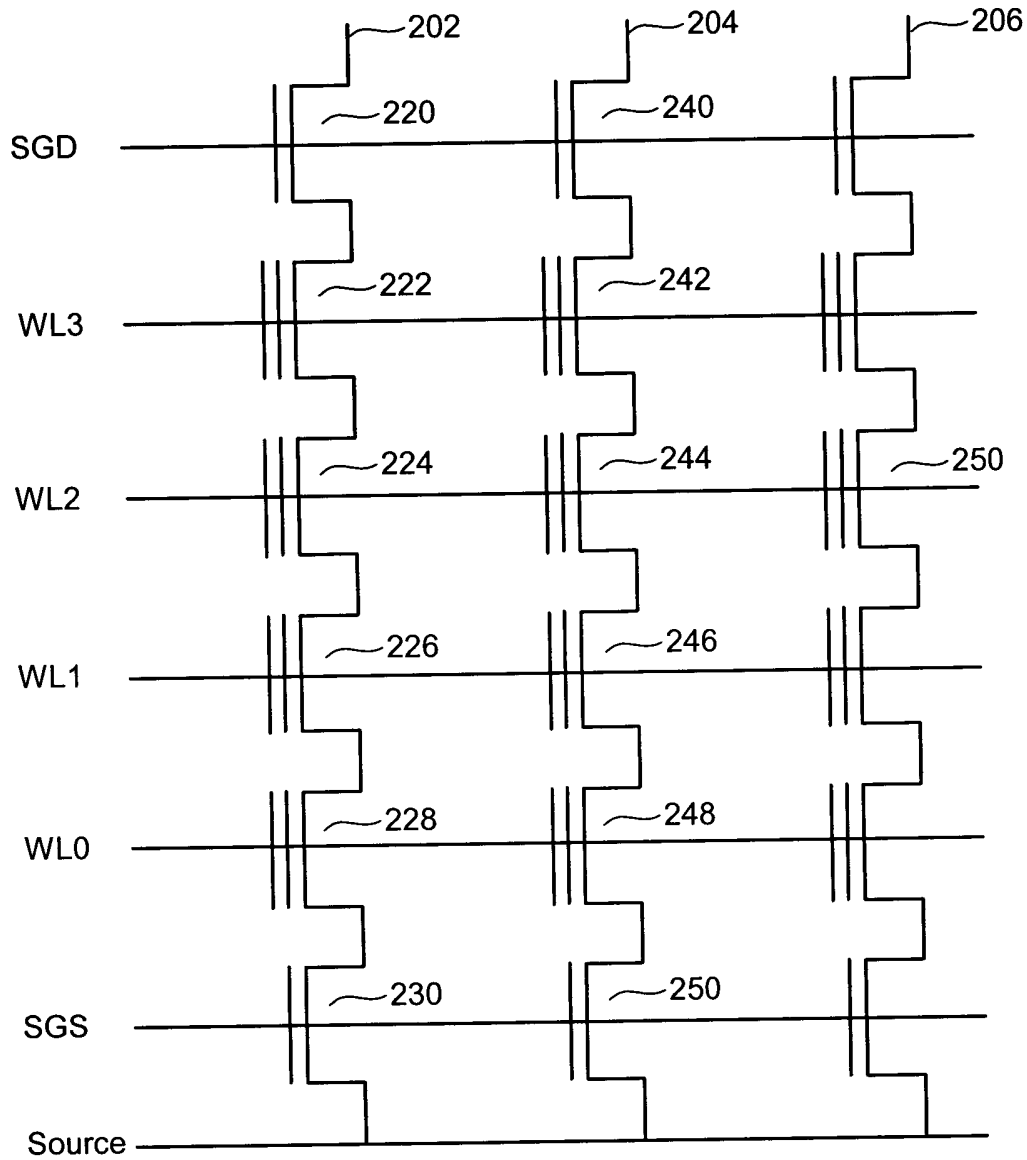
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Fig. 4



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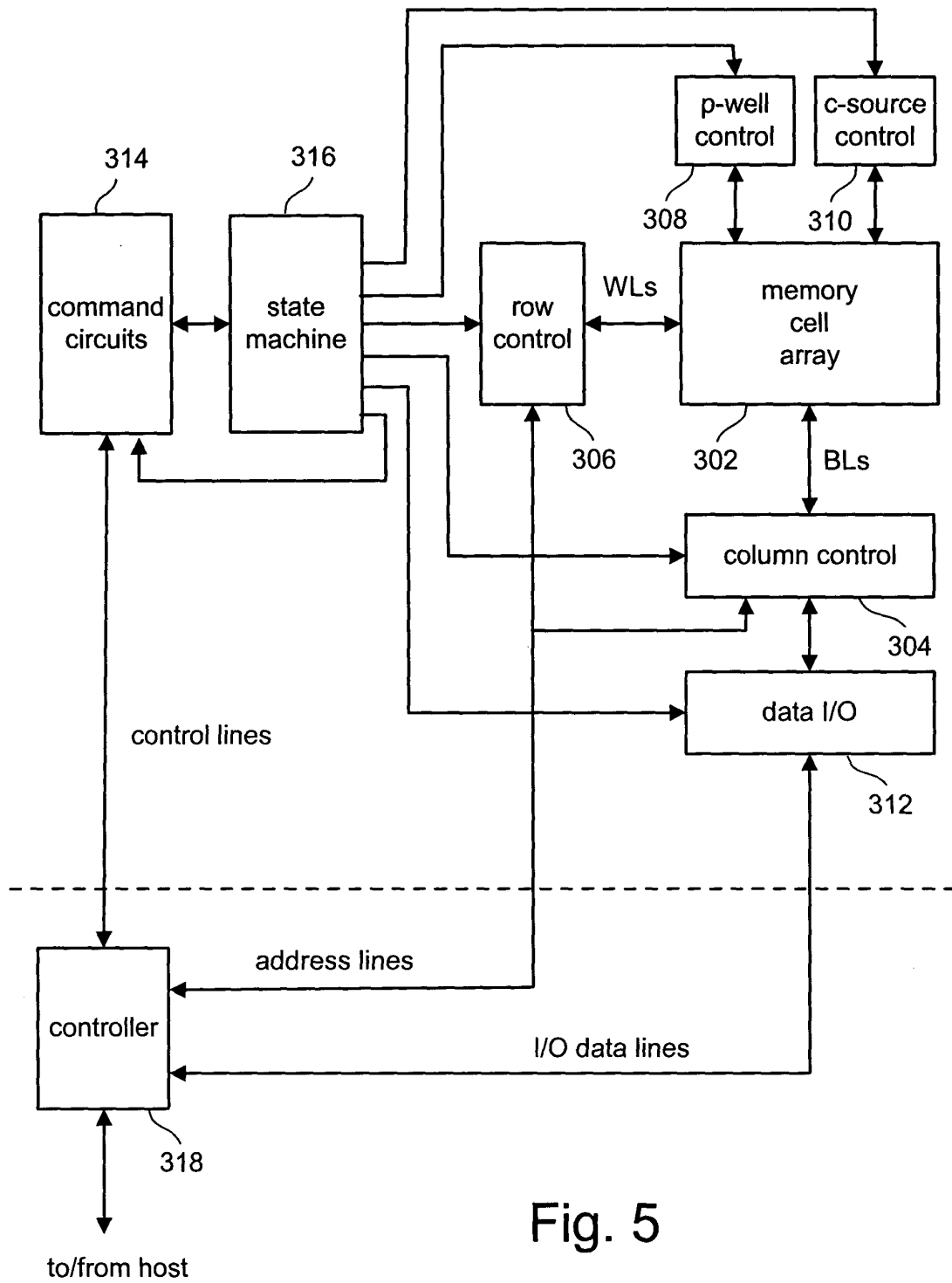


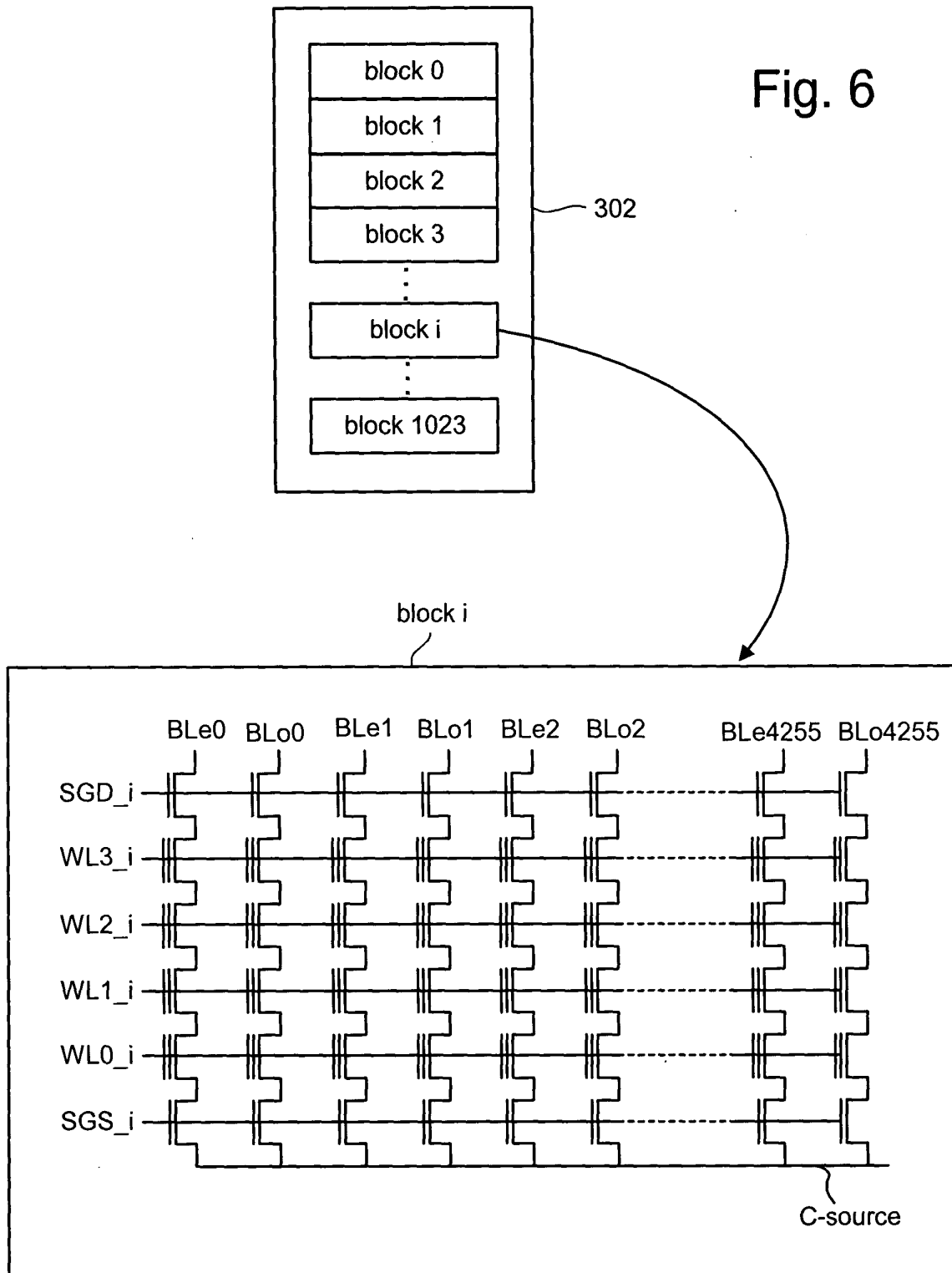
Fig. 5

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Fig. 7

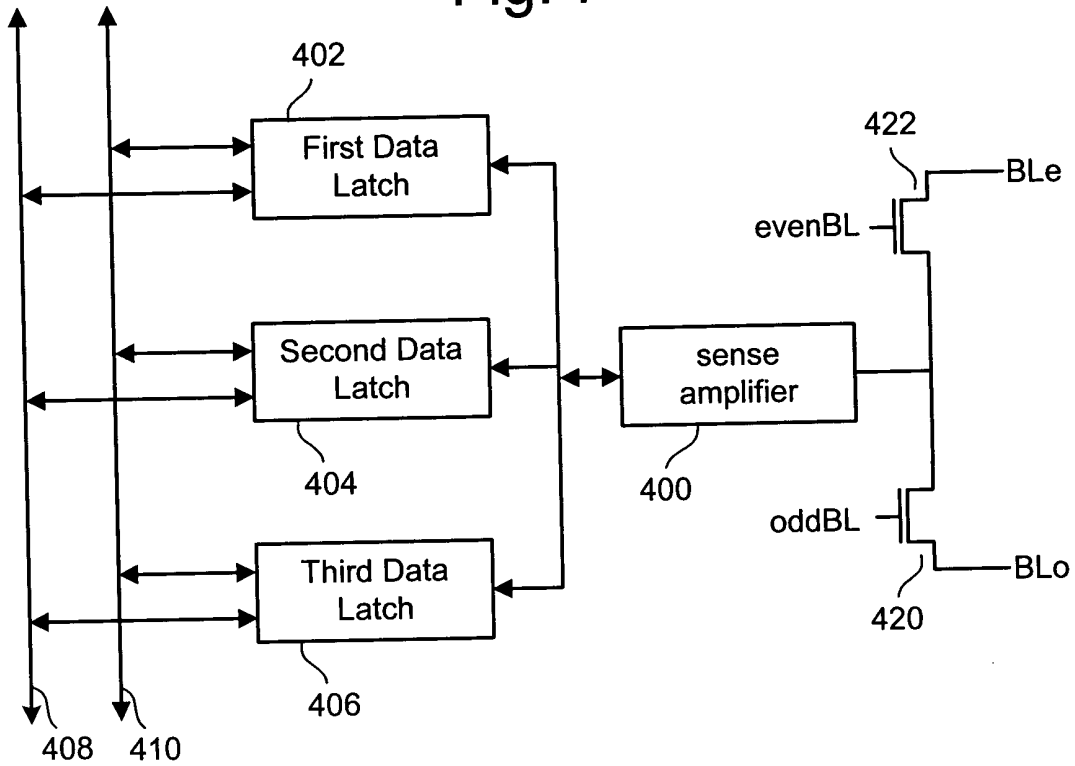
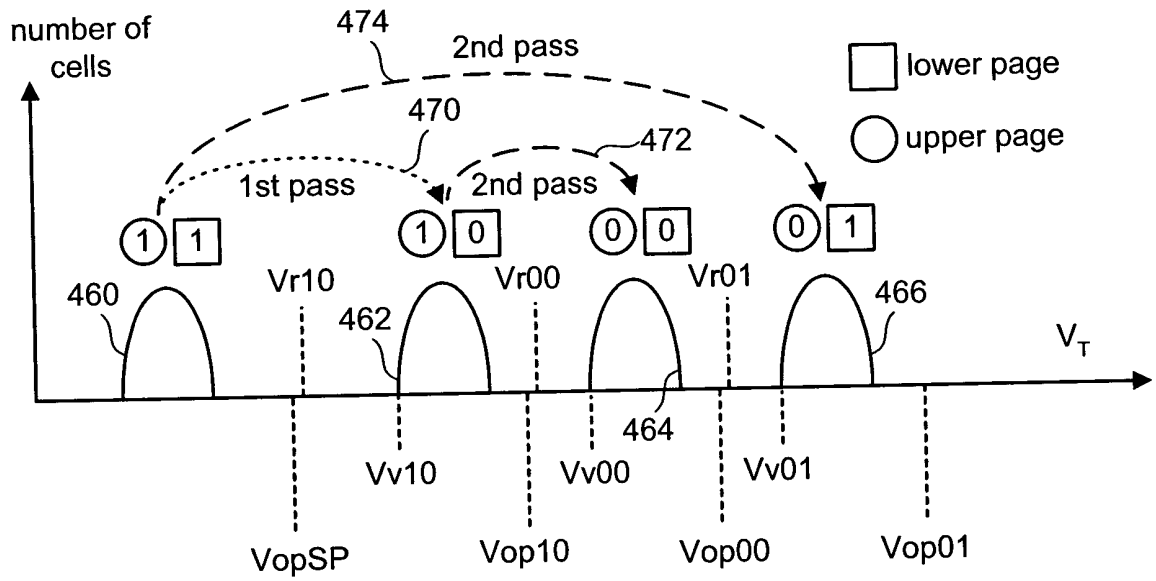


Fig. 8



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Fig. 9

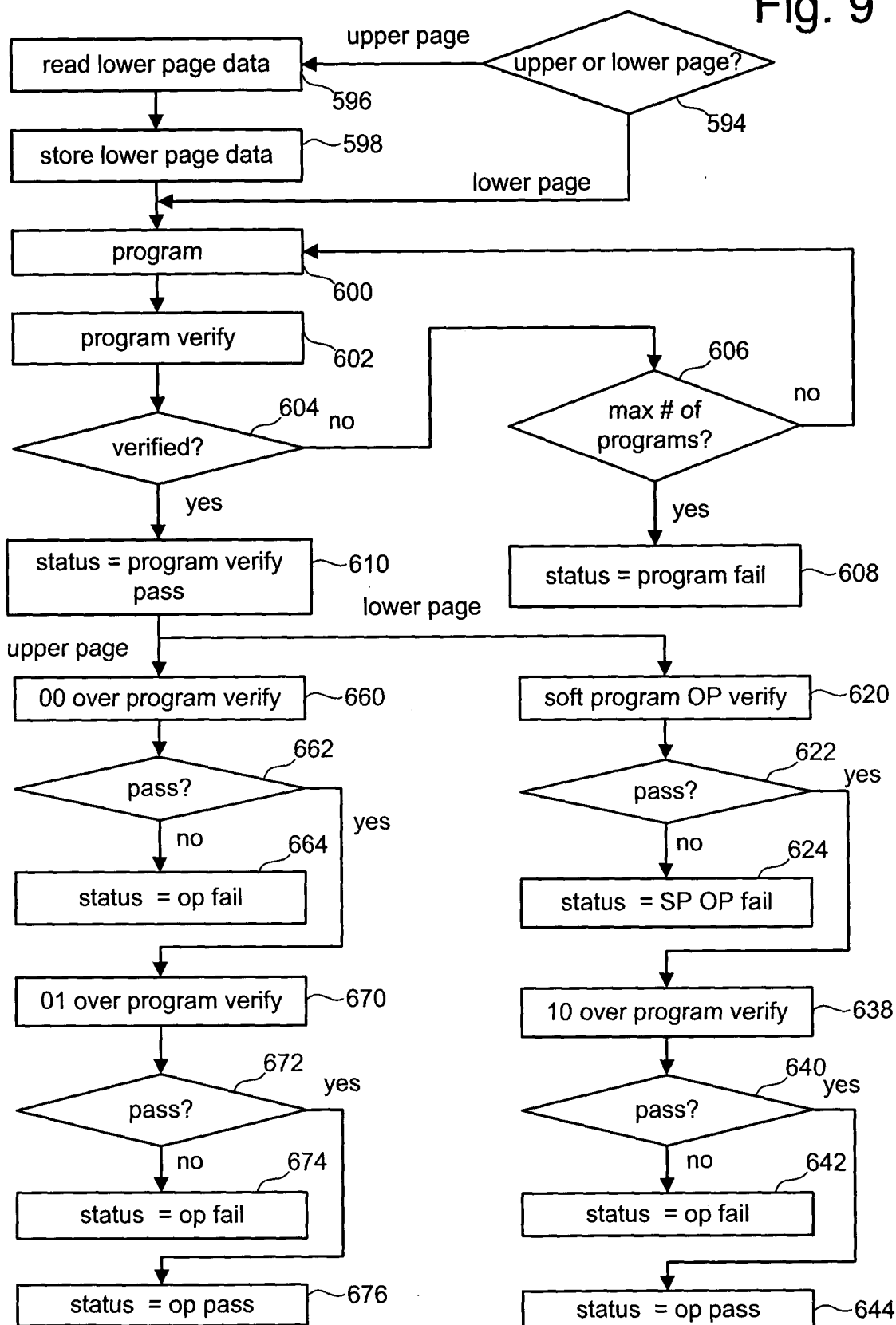


Fig. 10

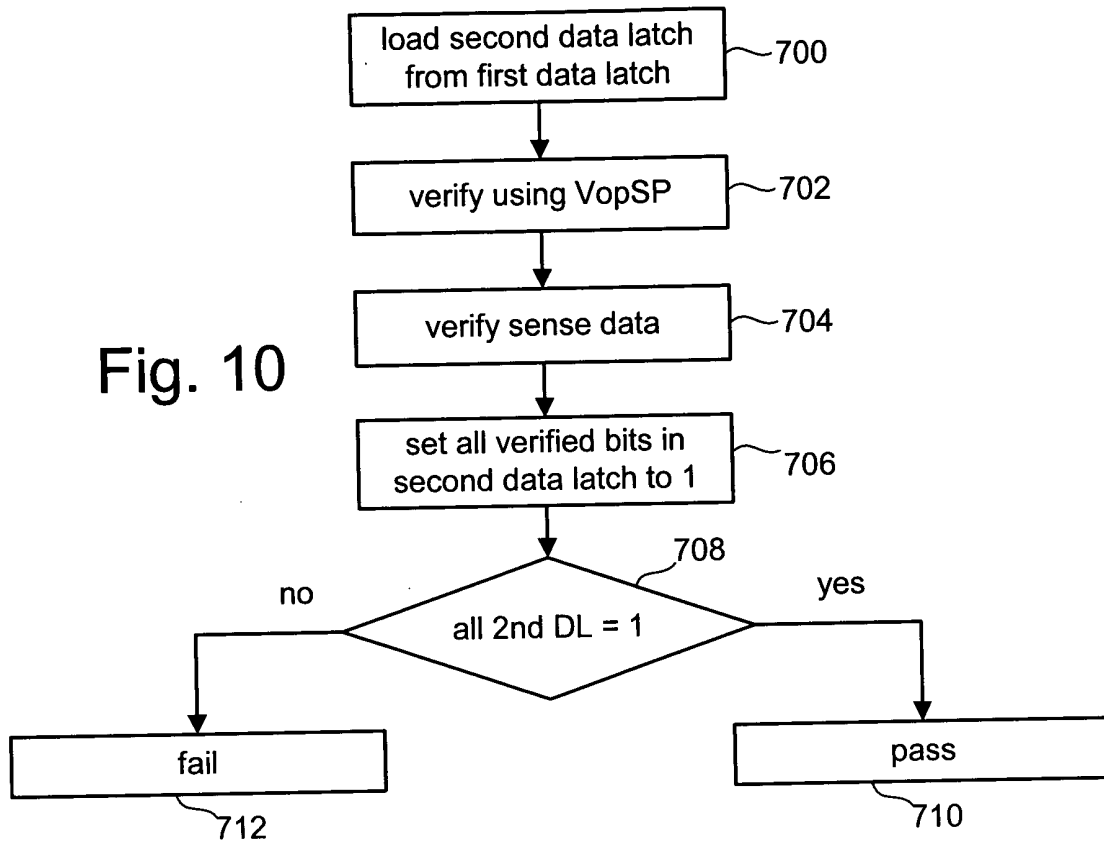
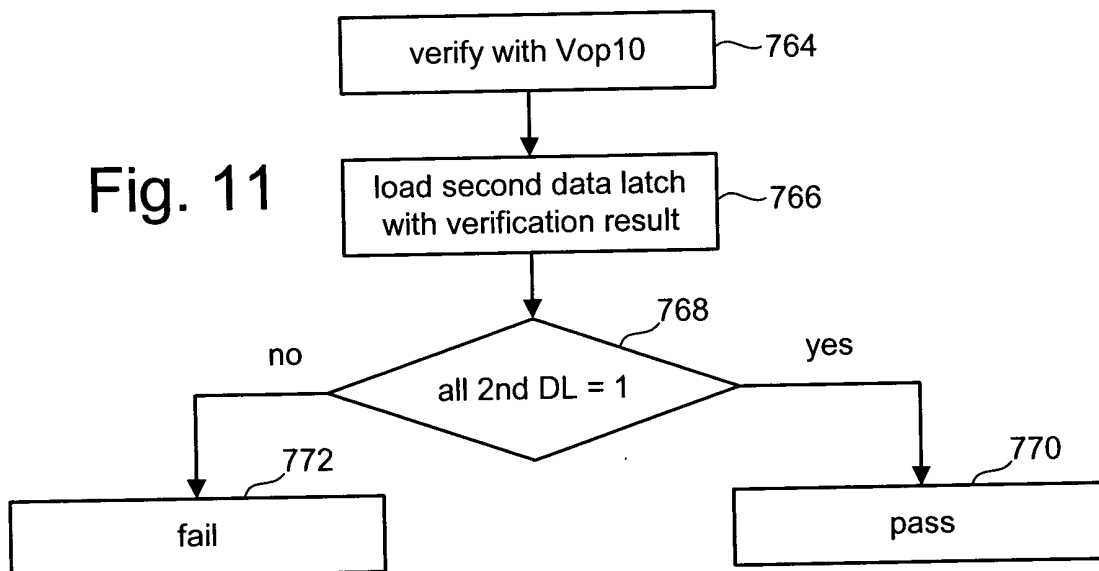


Fig. 11

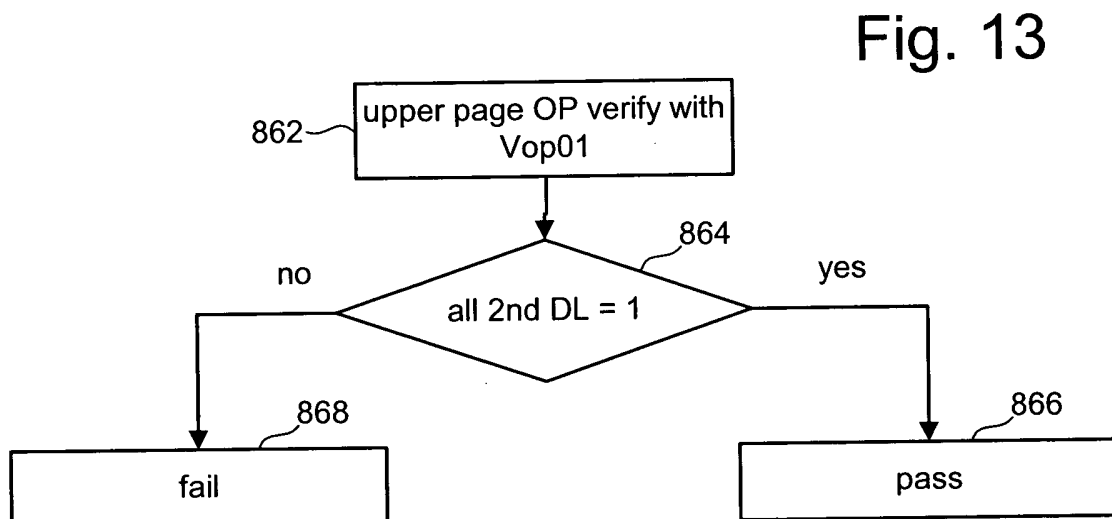
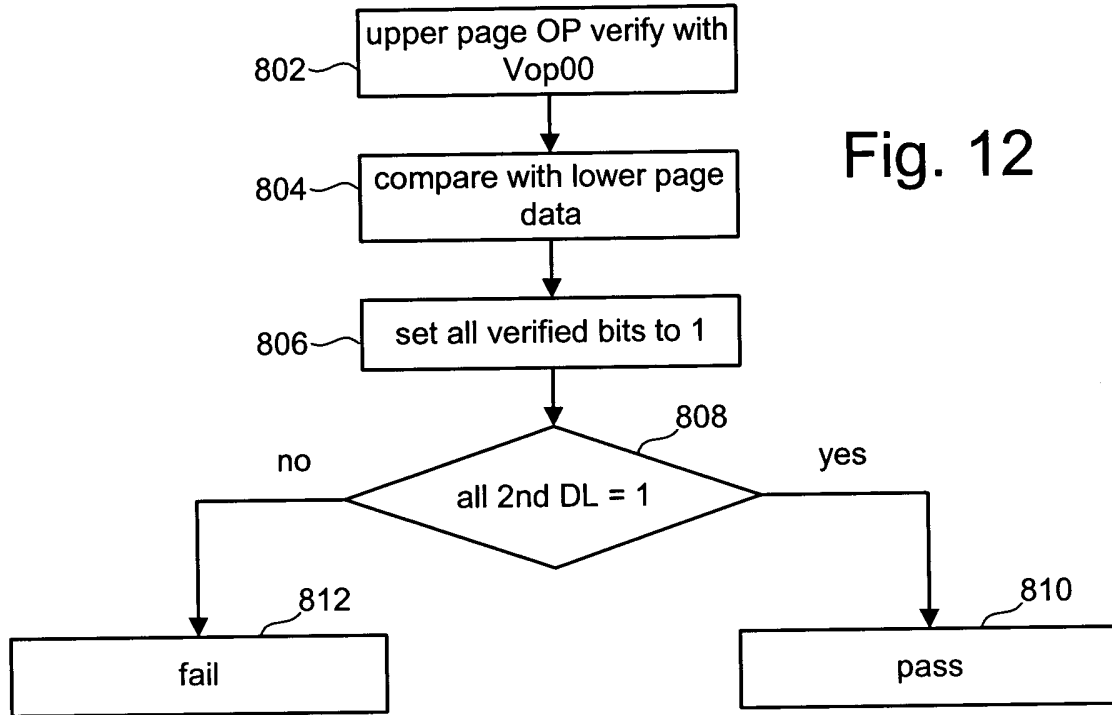


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Fig. 14A

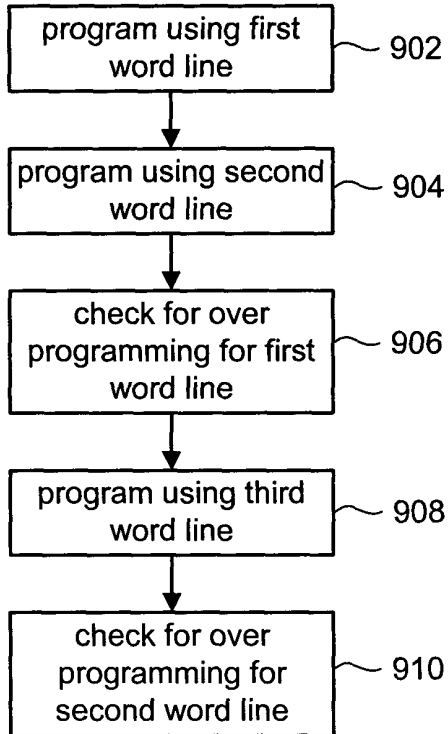
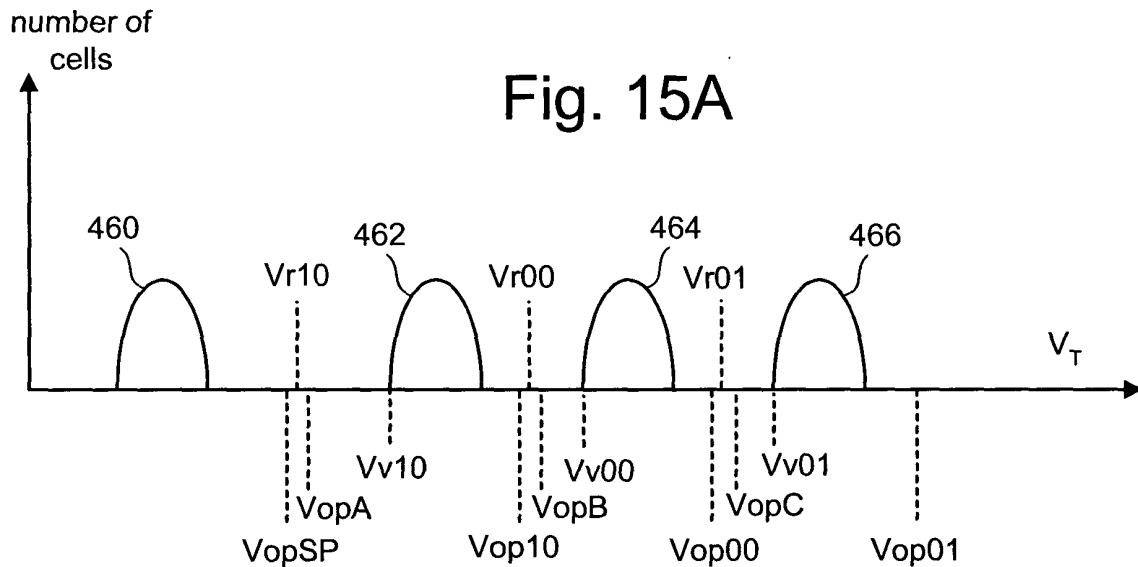
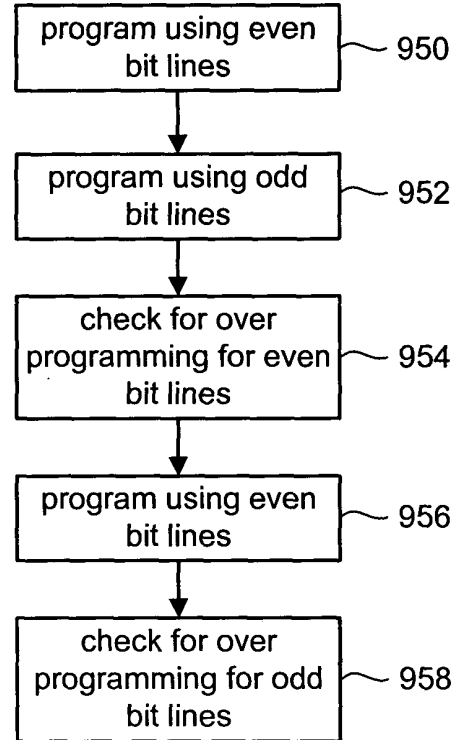


Fig. 14B



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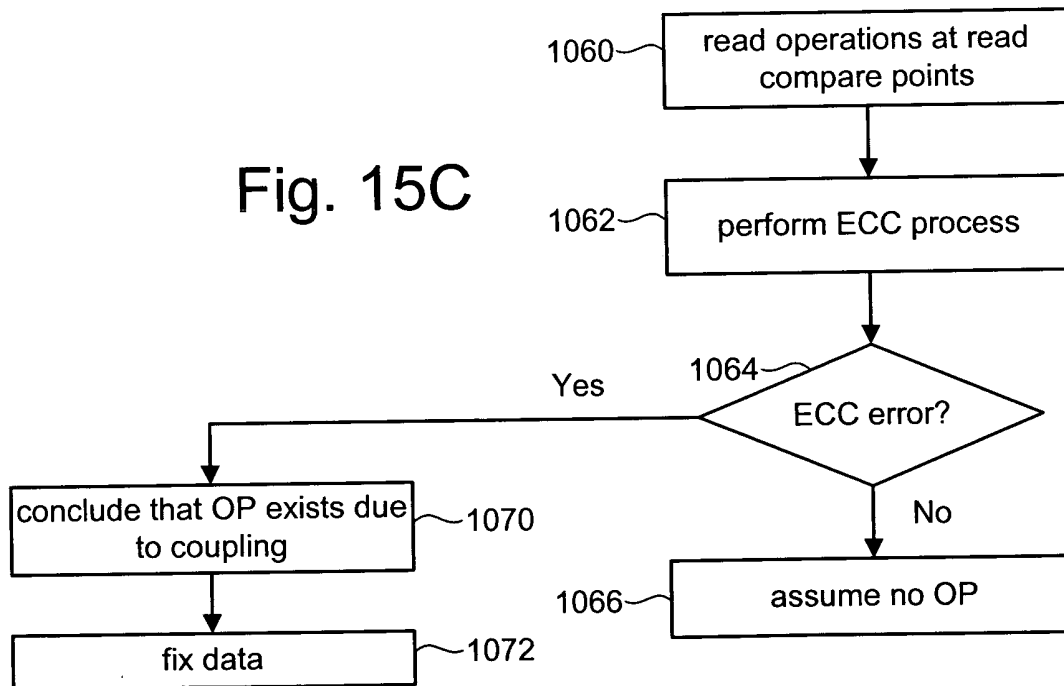
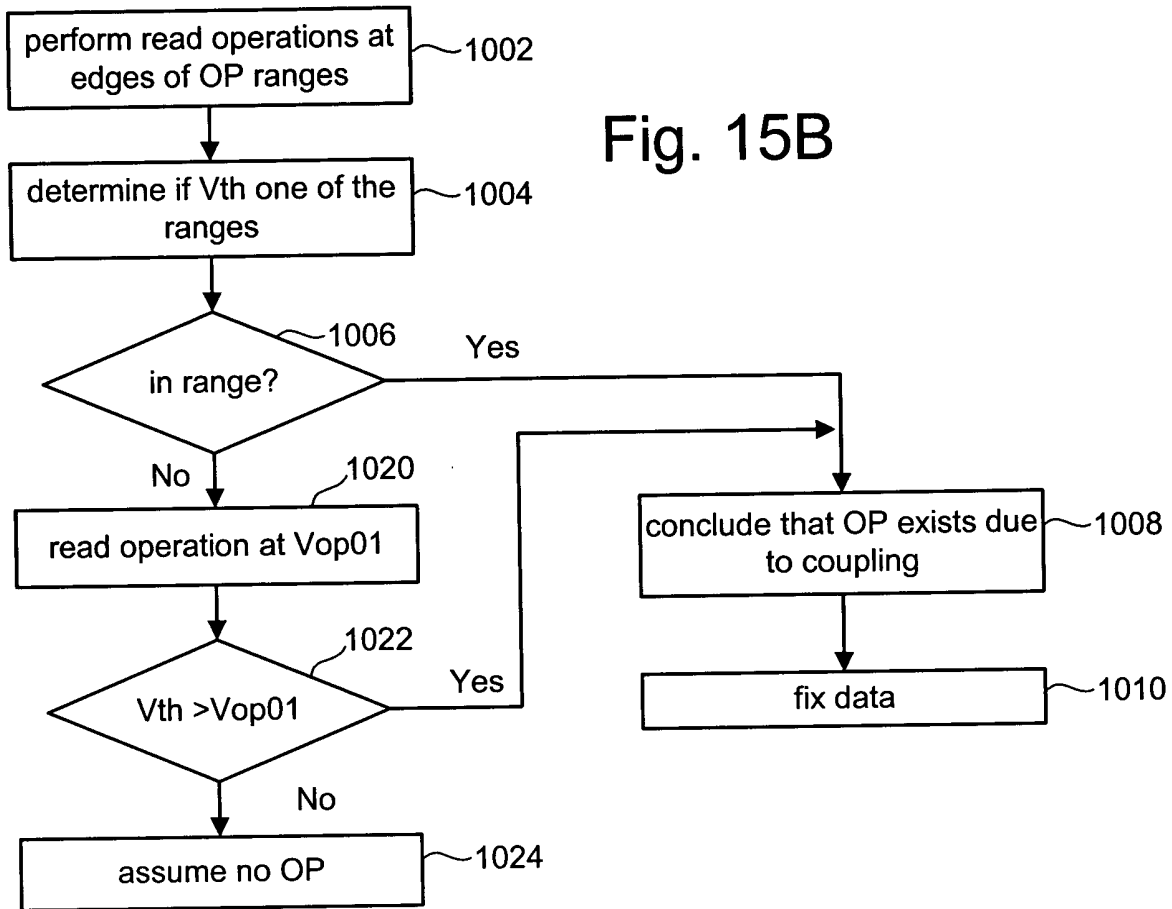


Fig. 16

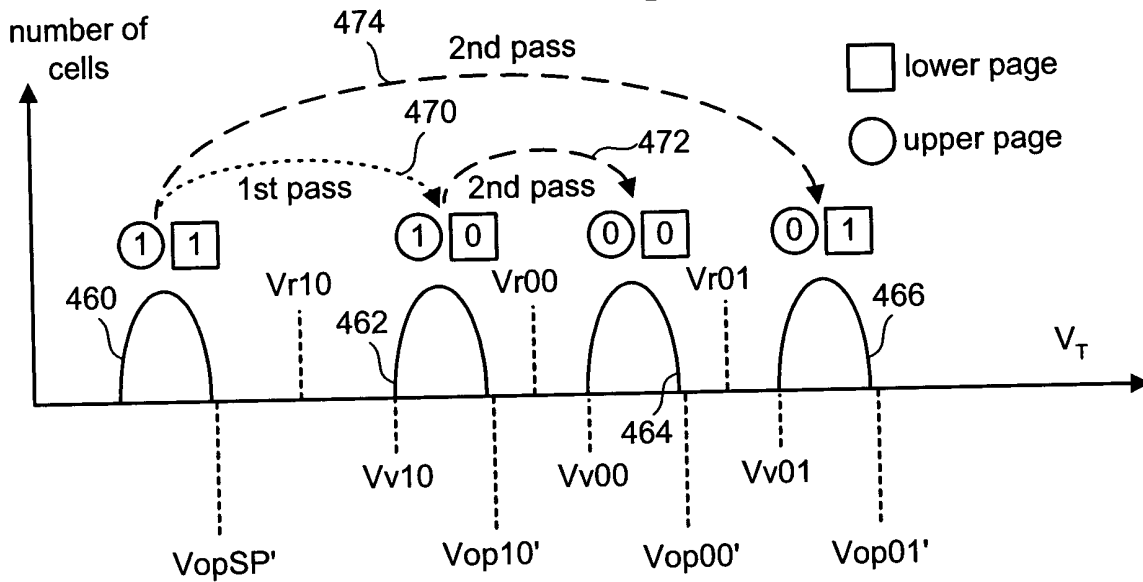


Fig. 17

	1	0
Read at VopSP'	1/0	0
Second Data Latch	1/0	0
First Data Latch	1	0
Test	Pass/Fail	Pass

Fig. 18

	11	10	00	01
Read at VopSP'	1/0	0	0	0
Second Data Latch	1/0	0	0	0
Third Data Latch	1	0	0	0
Test	Pass/Fail	Pass	Pass	Pass

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Fig. 19

	1	0
Read at Vop10'	1	1/0
Second Data Latch	1	1/0
First Data Latch	1	0
Test	Pass	Pass/Fail

Fig. 20

	11	10	00	01
Read at Vop10'	1	1/0	0	0
Second Data Latch	1	1/0	0	0
First Data Latch	1	1	0	0
Test	Pass	Pass/Fail	Pass	Pass

Fig. 21

	11	10	00	01
Read at Vop00'	1	1	1/0	0
Second Data Latch	1	1	1/0	0
Third Data Latch	1	0	0	1
Test	Pass	Pass	Pass/Fail	Pass

Fig. 22

	11	10	00	01
Read at Vop01'	1	1	1	1/0
Second Data Latch	1	1	1	1/0
Test	Pass	Pass	Pass	Pass/Fail